CLAIMS

1. A method for electroplating a metal layer on a semiconductor structure having recessed regions and non-recessed regions, comprising:

electroplating within a first current density range before the metal layer is planar above recessed regions of a first density; and

electroplating within a second current density range after the metal layer is planar above the recessed regions, wherein the second current range is greater than the first current range.

2. The method of claim 1, wherein the first current density range is between 0.5 mÅ/cm^2 and 5 mÅ/cm^2, and the second current density range is between 5 mÅ/cm^2 and 30 mÅ/cm^2.

3. The method of claim 1, wherein electroplating within the first current density range is carried out at a constant current density.

4. The method of claim 1, wherein electroplating within the first current density range is carried out at an increasing current density.

5. The method of claim 4, wherein the first current density increases linearly.

6. The method of claim 4, wherein the first current density increases non-linearly.

7. The method of claim 1, wherein electroplating within the first current density range includes decreasing the current density.

8. The method of claim 1, wherein electroplating within the second current density range is carried out at a constant current density.

9. The method of claim 1, wherein electroplating within the second current density range is carried out at an increasing current density.

10. The method of claim 9, wherein the second current density increases non-linearly.

11. The method of claim 1, wherein electroplating within the second current density range is carried out at a decreasing current density.

12. The method of claim 1, wherein the recessed regions of a first density include recesses with a size between 0.035 to 0.5 microns and spacing in the range of 0.035 to 0.5 microns, and

a large recess with a dummy structure having a size between 0.05 and 2.0 microns and spacing in the range 0.05 and 2.0 microns.

13. The method of claim 12, wherein the metal layer is electroplated above the regions of the first density until the metal layer is planar above the regions of the first density, and

electroplating over a region of second density until the metal layer is planar above the region of first density and the region of second density, wherein the region of second density is greater than the region of first density.

14. The method of claim 13, wherein after the metal layer is planar above the region of second density and the region of first density, electroplating at a third current density greater than the second current density.

15. The method of claim 1, wherein the metal layer is electroplated with an electrolyte fluid including an accelerator, suppressor, and leveler.

16. The method of claim 15, wherein the accelerator concentration is between 1.5 and 2.5 ml/liter, the suppressor concentration is between 7 and 9 ml/liter, and the leveler concentration is between 1.25 and 1.75 ml/liter.

17. The method of claim 1, further including controlling the grain size of the metal layer with additives in the electrolyte fluid.

18. The method of claim 17, wherein the additives include at least one of a brightener, accelerator, suppressor, and leveler

19. The method of claim 1, further including rotating the semiconductor structure with a chuck at a rotation speed of 50-200 rpm.

20. The method of claim 1, further including rotating the semiconductor structure with a chuck at a rotation speed of 125 rpm.

21. A method for electropolishing a metal layer on a semiconductor structure, comprising:

electropolishing a metal layer formed over recessed regions and non-recessed regions, wherein the metal layer is electropolished to a height less than the height of the non-recessed regions, and the non-recessed regions include a hard mask layer; and

removing at least a portion of the hard mask layer such that the height of the metal layer and the non-recessed regions are substantially planar.

22. The method of claim 21, wherein only a portion of the hard mask layer is removed.

23. The method of claim 21, wherein the hard mask layer is formed over a dielectric layer.

24. The method of claim 21, wherein the hard mask layer includes a sacrificial layer and an etch stop layer.

25. The method of claim 24, wherein the metal layer is electropolished to a height substantially planar with the etch stop layer included in the mask layer.

26. The method of claim 25, wherein the sacrificial layer is removed with an etch having a higher selectivity for the sacrificial layer than the etch stop layer included in the hard mask layer.

27. The method of claim 21, further including planarizing the metal layer formed over the semiconductor structure prior to electropolishing.

28. The method of claim 27, wherein the metal layer is planarized by a chemical mechanical polishing process.

29. The method of claim 21, wherein the semiconductor structure includes dummy structures formed in the recessed regions to increase the planarity of the formed metal layer.

30. The method of claim 21, wherein the non-recessed regions are etched.

31. The method of claim 21, wherein the height of the metal layer is electropolished to a height between 200 Å and 1000 Å less than the height of the non-recessed regions of the structure.

32. The method of claim 21, wherein the height of the metal layer is electropolished to a height of 500 Å less than the height of the non-recessed regions of the structure.

33. The method of claim 21, wherein the non-recessed regions of the structure removed include a barrier layer and an etch stop layer.

34. The method of claim 21, wherein a dielectric layer included in the non-recessed regions of the structure is not etched when etching.

35. The method of claim 21, further including depositing a polymer layer over the metal layer and the non-recessed regions of the structure.

36. The method of claim 21, further including depositing a dielectric layer over the metal layer and the non-recessed regions of the structure.

37. The method of claim 36, further including forming a second semiconductor structure including recessed regions and non-recessed regions over the dielectric layer.

38. A method for forming a metal layer on a semiconductor structure, comprising:
electroplating a metal layer on a semiconductor structure with an electrolyte fluid;
introducing additives to control a grain size of the metal layer in the electrolyte fluid; and
electropolishing the metal layer before such time that the grain size increases to one micron.

39. The method of claim 38, wherein the metal layer is plated with a grain size of less than 200 Å.

40. The method of claim 38, wherein the additive includes a brightener.

41. The method of claim 38, wherein the additive includes an accelerator.

42. The method of claim 41, wherein the accelerator is between 1.5 ml/liter and 2.5 ml/liter.

43. The method of claim 38, wherein the additive includes a suppressor.

44. The method of claim 43, wherein the suppressor is between 7 ml/liter and 9 ml/liter.

45. The method of claim 38, wherein the additive includes a leveler.

46. The method of claim 45, wherein the leveler is between 1.25 ml/liter and 1.75 ml/liter.

47. The method of claim 38, wherein the additive includes at least one of a brightener, accelerator, suppressor, and a leveler.

48. The method of claim 38, further including electropolishing the metal layer, wherein a time between electroplating and electropolishing the metal layer is determined to further control the grain size of the metal layer.

49. The method of claim 38, further including electropolishing the metal layer within 20 hours of electroplating.

50. The method of claim 38, further including electropolishing the metal layer within 5 hours of electroplating.

51. A method for forming a metal layer on a semiconductor structure, comprising:

electroplating a metal layer on a semiconductor structure;

electropolishing the metal layer on the semiconductor structure after electroplating the metal layer; and

annealing the metal layer after it has been electropolished, wherein the annealing increases a grain size of the metal layer.

52. The method of claim 51, further including chemical mechanical polishing the metal layer after electroplating and before electropolishing the metal layer.

53. The method of claim 52, wherein the chemical mechanical polishing planarizes the metal layer.

54. The method of claim 51, wherein the metal layer includes copper.

55. The method of claim 51, wherein the metal layer is plated on a metal seed layer less than 1500 Å in thickness.

56. The method of claim 51, wherein the metal layer is plated on a 100 Å thick metal seed layer.

57. The method of claim 51, wherein the annealing includes heating the metal layer with an infrared source.

58. The method of claim 51, wherein the annealing includes heating the metal layer with an oven

59. The method of claim 51, wherein the annealing includes heating the metal layer between 100 °C and 300 °C.

60. The method of claim 51, wherein the annealing includes heating the metal layer at approximately 150 °C.

61. The method of claim 51, wherein a time between electroplating and electropolishing is determined to control the grain size of the metal layer.

62. The method of claim 61, wherein the time is less than 20 hours.

63. The method of claim 61, wherein the time is less than 5 hours.

64. The method of claim 61, wherein the time is determined to have a grain size of less than 100Å when electropolishing.

65. The method of claim 61, wherein the time is determined to have a grain size of less than 500Å when electropolishing.

66. The method of claim 61, wherein the time is determined to have a grain size of less than 1000Å when electropolishing.

67. A method for electropolishing a metal layer on a semiconductor wafer, comprising:

directing a stream of electrolyte fluid to a metal layer on a semiconductor wafer;

moving the stream of electrolyte fluid and the wafer relative to each other; and

applying an alternating forward and reverse voltage between the nozzle and the metal layer, wherein

a first transition is made between the forward and reverse voltage when the stream of electrolyte fluid is adjacent an interface between the metal layer of a first conductivity and a material of second conductivity, and

the first conductivity is different than the second conductivity.

68. The method of claim 67, further including a second transition between the forward and reverse voltage when the stream of electrolyte fluid is over the metal layer.

69. The method of claim 68, wherein the first transition and second transition reduce overpolishing of the metal layer.

70. The method of claim 67, wherein the material of second conductivity is a barrier layer.

71. The method of claim 67, wherein the metal layer includes copper and the material of second conductivity is a barrier layer.

72. The method of claim 67, wherein the first conductivity is greater than the second conductivity.

73. The method of claim 67, wherein the alternating forward and reverse voltage is pulsed at a frequency in the range of 100 kHz and 100 MHz.

74. The method of claim 67, wherein the alternating forward and reverse voltage is pulsed at a frequency of approximately 3 MHz.

75. The method of claim 67, wherein the forward voltage pulse duration is between a range of 20 and 80 percent of the reverse voltage pulse.

76. The method of claim 67, wherein the forward voltage pulse duration is approximately 50 percent of the reverse voltage pulse.

77. The method of claim 67, wherein the relative velocity of the wafer and the stream of electrolyte fluid is between 100 mm/sec and 2,000 mm/sec.

78. The method of claim 67, wherein the relative velocity of the wafer and the stream of electrolyte fluid is approximately 500 mm/sec.